

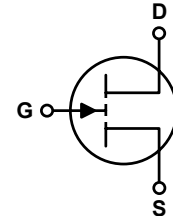
INN040FQ043A

1. General Description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 3 mm x 4 mm package size.

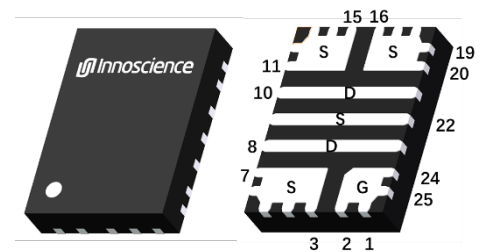
2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint



3. Applications

- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver



4. Key Performance Parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	40	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	4.3	m Ω
$Q_{G,typ}$ @ $V_{DS} = 20\text{ V}$	6.2	nC
$I_{DS,Pulse}$	160	A
$Q_{OSS}@ V_{DS} = 20\text{ V}$	14	nC

5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
1, 2, 24, 25	Gate	Driver Gate
3-7, 9, 11-20, 22	Source	Source
8, 10, 21, 23	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040FQ043A	FCQFN 3x4	D17

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6. Maximum Ratings

at $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
I_D	Continuous current	24	A
	Pulsed ($25\text{ }^\circ\text{C}$, $T_{Pulse} = 300\text{ }\mu\text{s}$)	160	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
P_{tot}	Power dissipation ($T_{c, bottom} = 25\text{ }^\circ\text{C}$)	43	W
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^\circ\text{C}$

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC_top}$	Thermal Resistance, Junction to Case (top)	26.2	°C/W	
$R_{\theta JC_bot}$	Thermal Resistance, Junction to Case (bottom)	2.9	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	45.9	°C/W	
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric Characteristics

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	40			V	$V_{GS} = 0\text{ V}$, $I_D = 500\text{ }\mu\text{A}$
I_{DSS}	Drain Source Leakage			100	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 32\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage		3	80	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Forward Leakage		50	500	μA	$V_{GS} = 5\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$
	Gate-to-Source Reverse Leakage		1	20	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.7		2.4	V	$V_{DS} = V_{GS}$, $I_D = 7\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance		3	4.3	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$, $I_D = 15\text{ A}$
V_{SD}	Source-Drain Forward Voltage		1.9		V	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{iss}	Input Capacitance		805		pF	V _{GS} = 0 V, V _{DS} = 20 V
C _{oss}	Output Capacitance		428			
C _{rss}	Reverse Transfer Capacitance		13			
C _{oss(er)}	Energy Related Coss		600			V _{GS} = 5 V, V _{DS} = 20 V, I _D =15 A
C _{oss(tr)}	Time Related Coss		703			
R _G	Gate resistance		1.7		Ω	f = 1 MHz
Q _G	Total Gate Charge		6.2	8.5	nC	V _{GS} = 5 V, V _{DS} = 20 V, I _D =15 A
Q _{GS}	Gate to Source Charge		1.4			V _{DS} = 20 V, I _D = 15 A
Q _{GD}	Gate to Drain Charge		0.8			
Q _{G(TH)}	Gate Charge at Threshold		0.9			
Q _{OSS}	Output Charge		14			V _{GS} = 0 V, V _{DS} = 0 V to 20 V

9. Electric Characteristics Diagrams

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Figure 1 Typical Output Characteristics ($T_J = 25\text{ }^\circ\text{C}$)

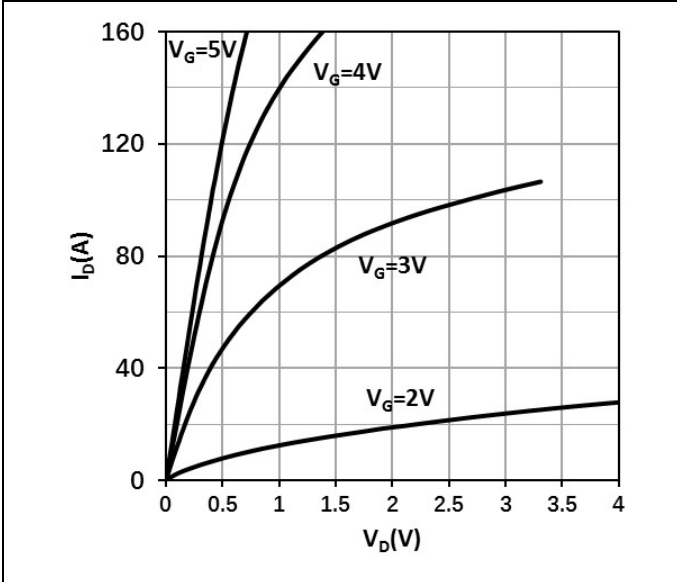


Figure 2 Typical Output Characteristics ($T_J = 125\text{ }^\circ\text{C}$)

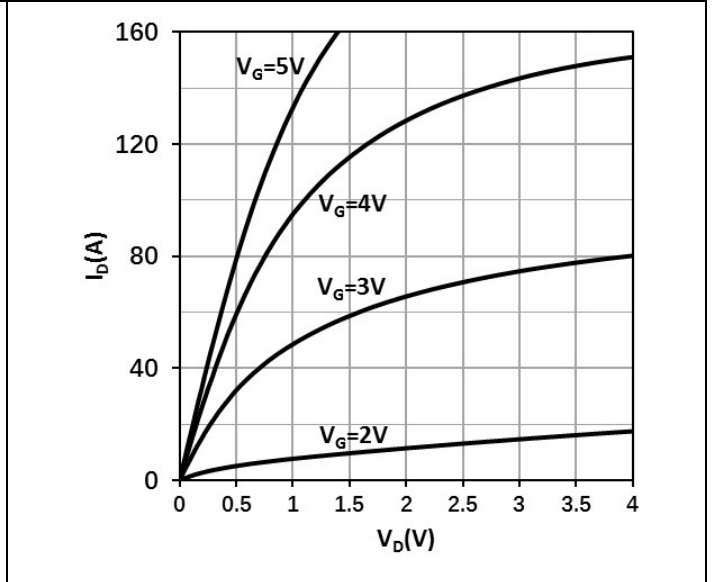


Figure 3 Typ. Drain On-state Resistance ($T_J = 25\text{ }^\circ\text{C}$)

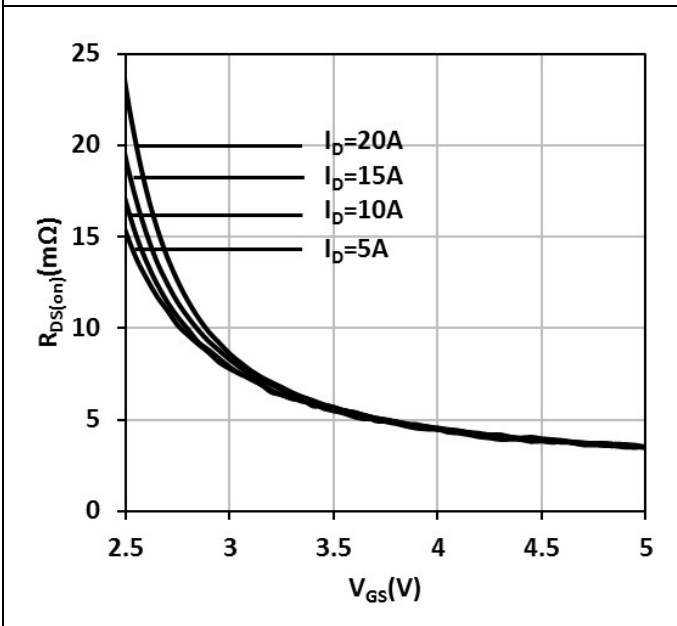


Figure 4 Typ. Drain On-state Resistance ($T_J = 125\text{ }^\circ\text{C}$)

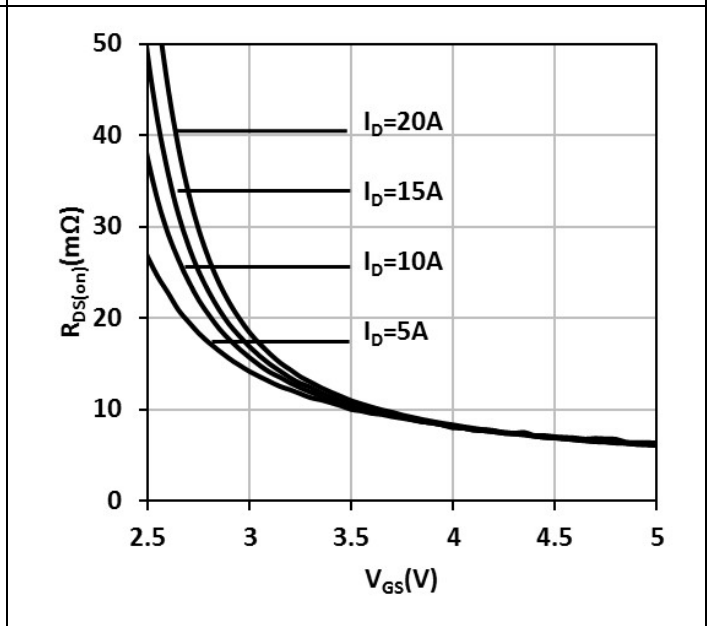


Figure 5 Typical On Resistance vs. Temperature

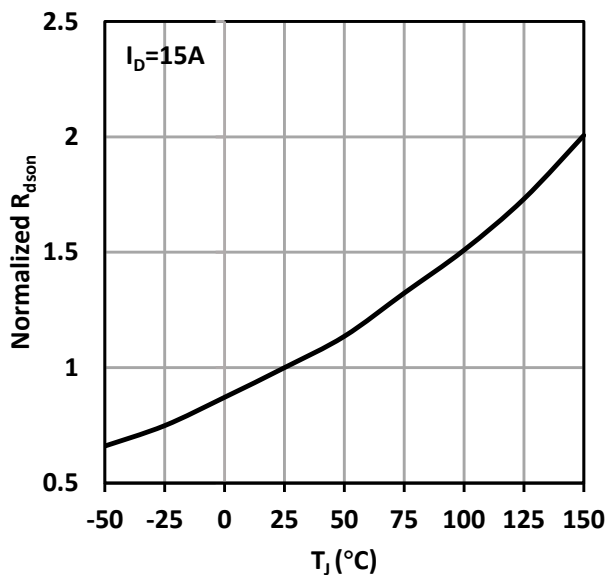


Figure 6 Typical Transfer Characteristics

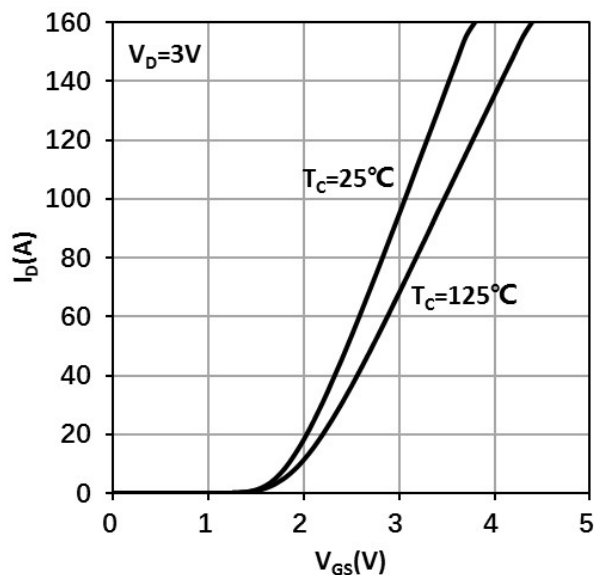


Figure 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 25^\circ C$)

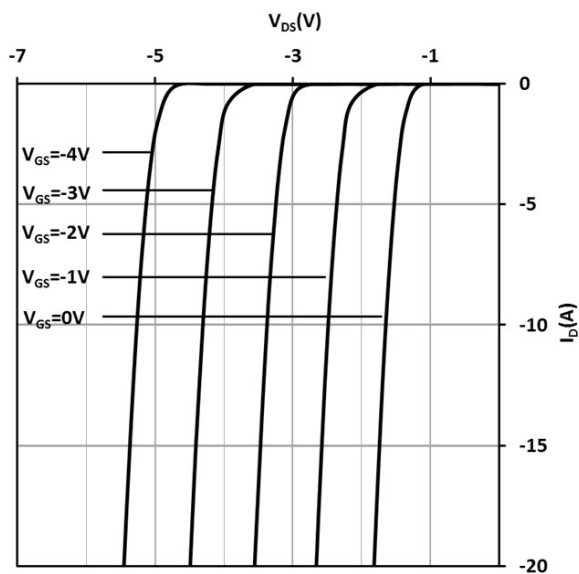


Figure 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 25^\circ C$)

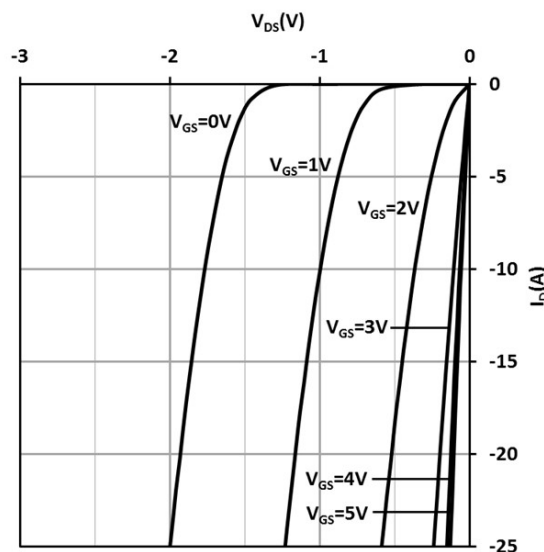


Figure 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 125\text{ }^\circ\text{C}$)

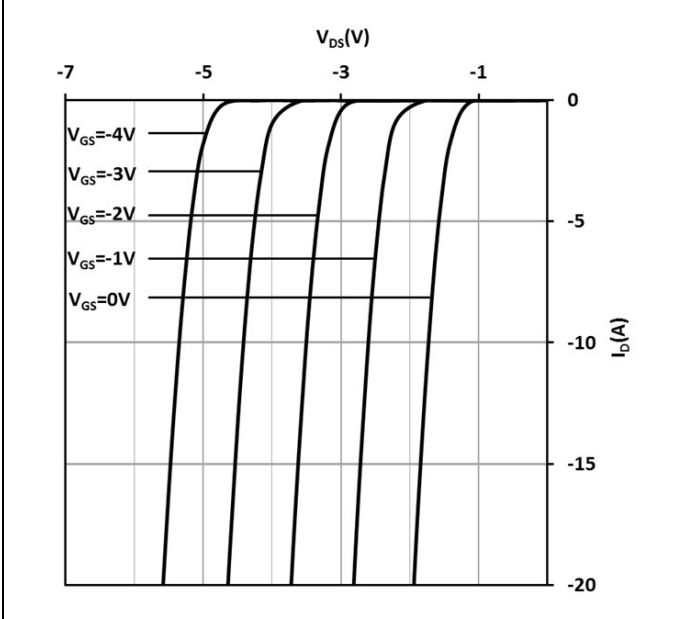


Figure 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 125\text{ }^\circ\text{C}$)

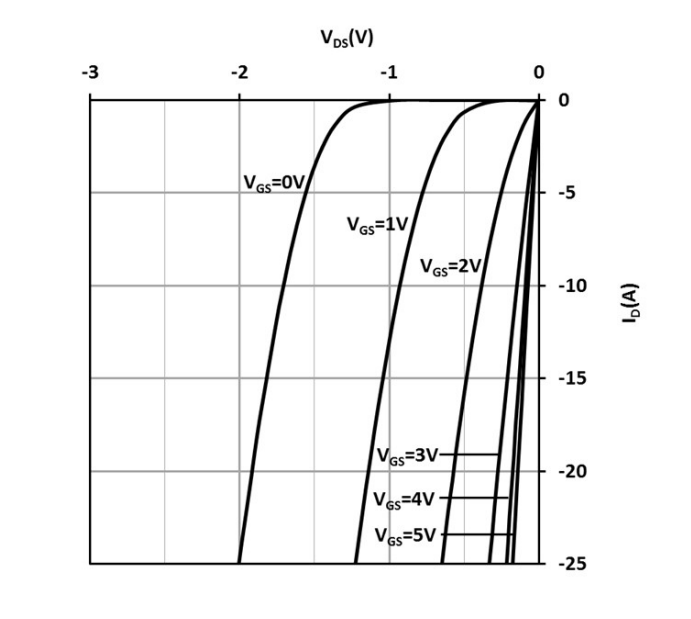


Figure 11 Typ. Capacitances Characteristics

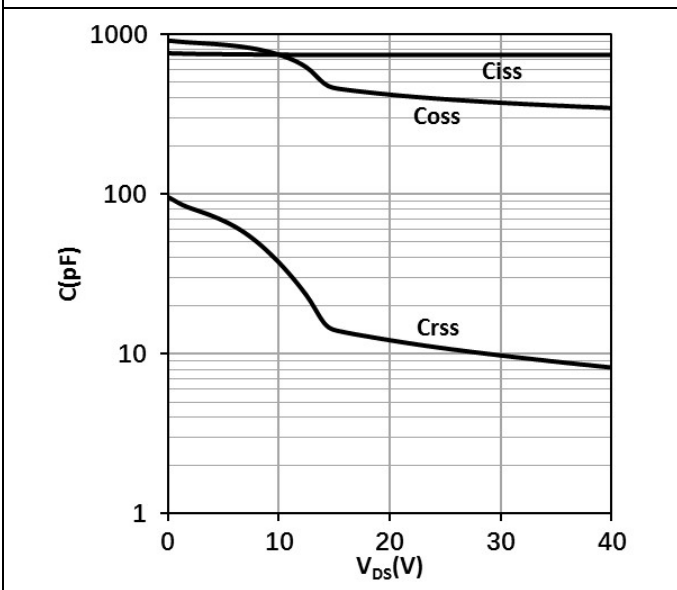


Figure 12 Typ. Gate Charge

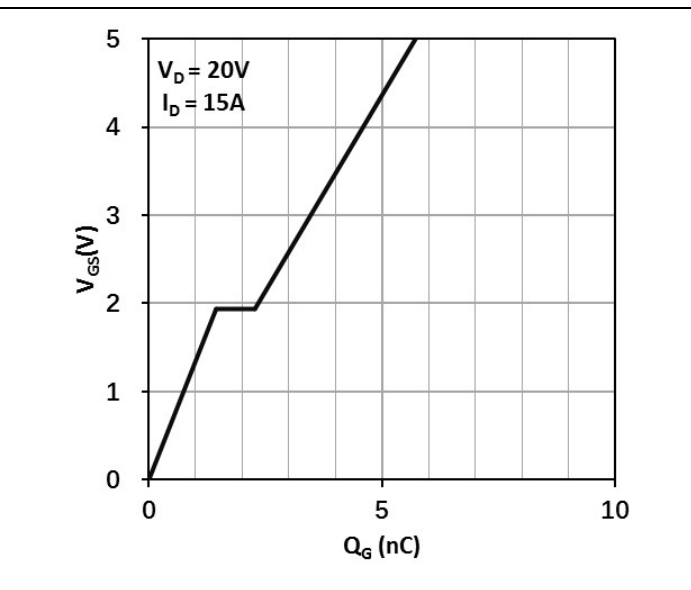


Figure 13 Normalized Threshold Voltage vs. Temp.

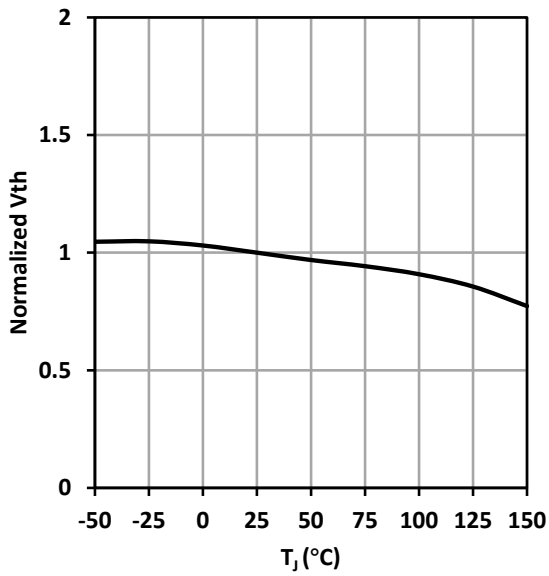


Figure 14 Output Charge

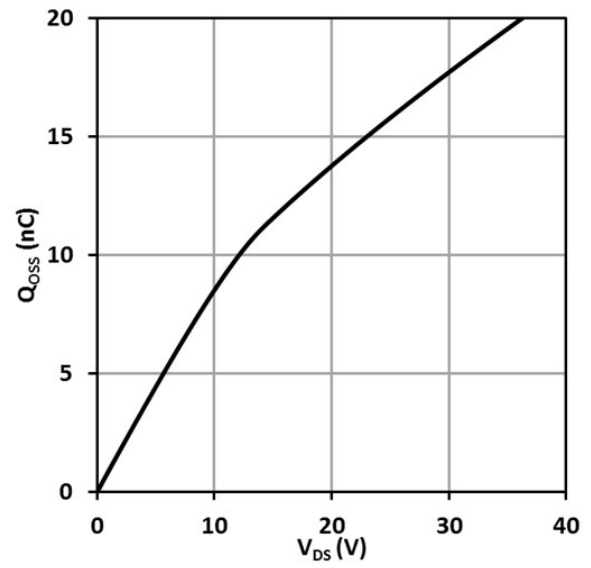


Figure 15 Output Capacitance Stored Energy

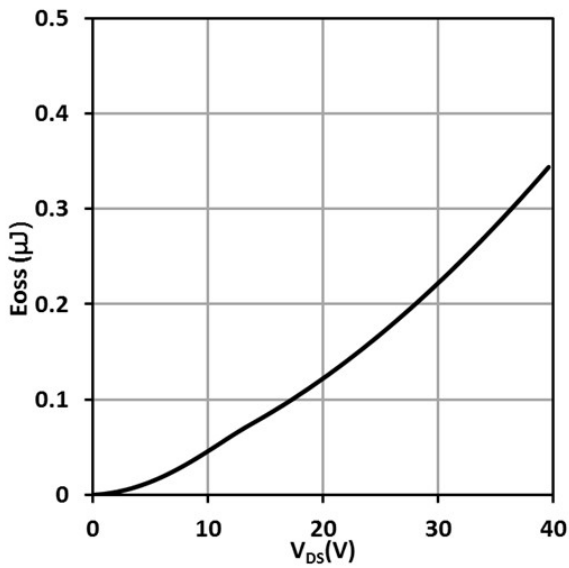


Figure 16 Power Dissipation

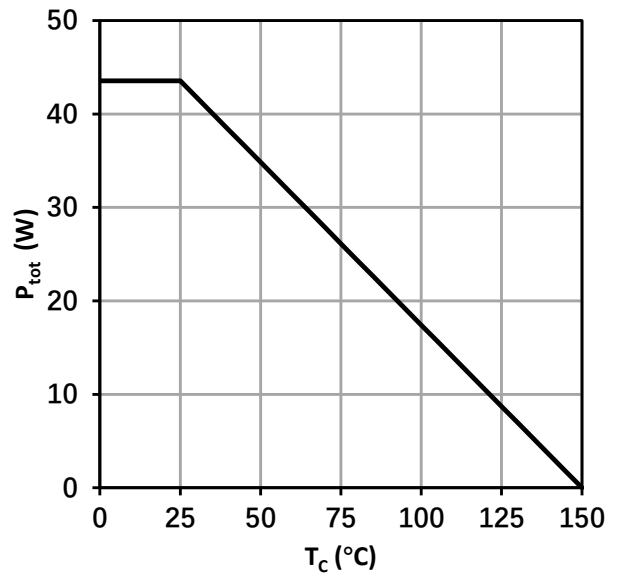


Figure 17 Safe Operating Area

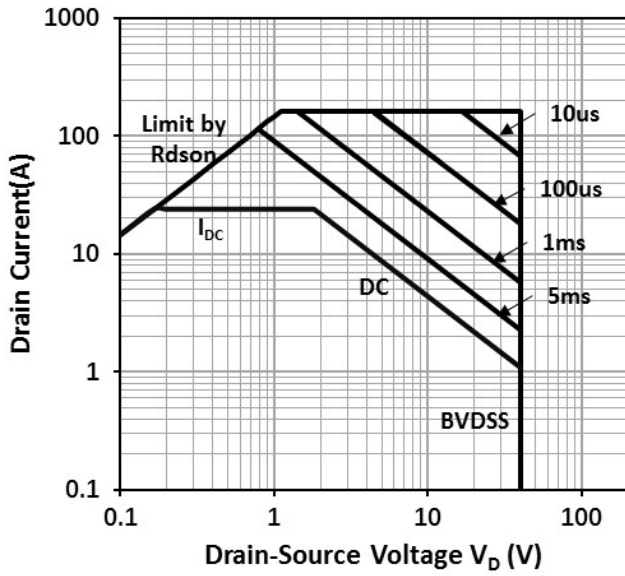
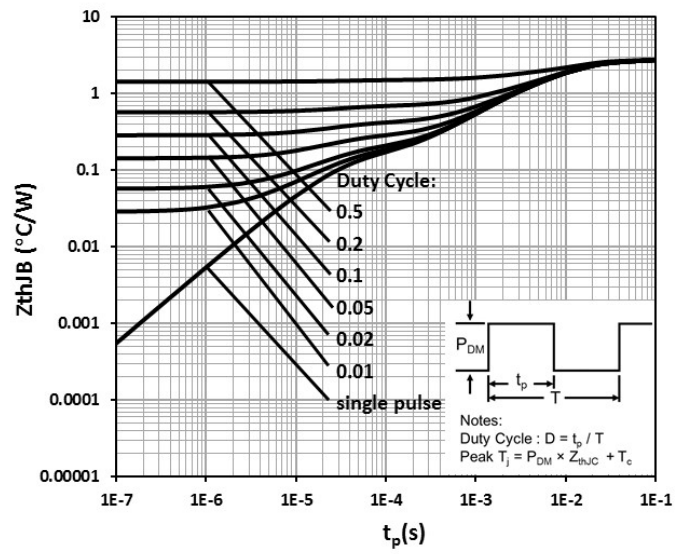
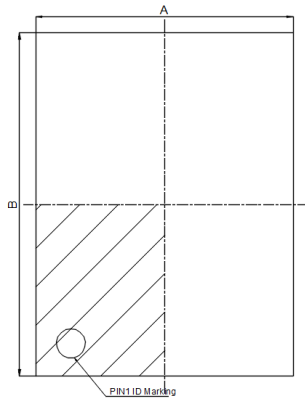


Figure 18 Max. Transient Thermal Impedance

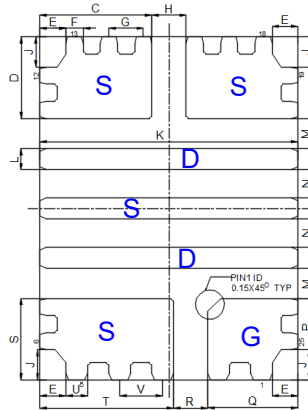


10. Package Outlines

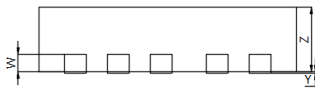
Package Reference



TOP VIEW



BOTTOM VIEW



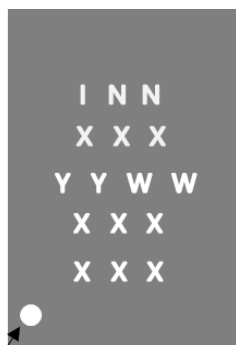
SIDE VIEW

NOTE:

- 1) ALL DIMENSION ARE IN MILLIMETERS.
- 2) BOTTOM VIEW IS FT TESTER SIDE VIEW.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) COMPLIES WITH JEDEC MO-220.
- 5) DRAWING IS NOT TO SCALE.

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	2.9	3.0	3.1	
B	3.9	4.0	4.1	
C	1.2	1.3	1.4	2X
D	0.85	0.95	1.05	2X
E	0.3 REF			4X
F	0.15	0.2	0.25	14X
G	0.4 BASIC			8X
H	0.35	0.4	0.45	
J	0.35 REF			4X
K	2.9	3.0	3.1	3X
L	0.20	0.25	0.30	3X
M	0.3	0.35	0.4	4X
N	0.275	0.325	0.375	2X
P	0.85	0.95	1.05	
Q	0.95	1.05	1.15	
R	0.35	0.4	0.45	
S	0.85	0.95	1.05	
T	1.45	1.55	1.65	
U	0.2	0.25	0.3	5X
V	0.5 BASIC			3X
W	0.203 REF			
Y	0	0.02	0.05	
Z	0.65	0.75	0.85	

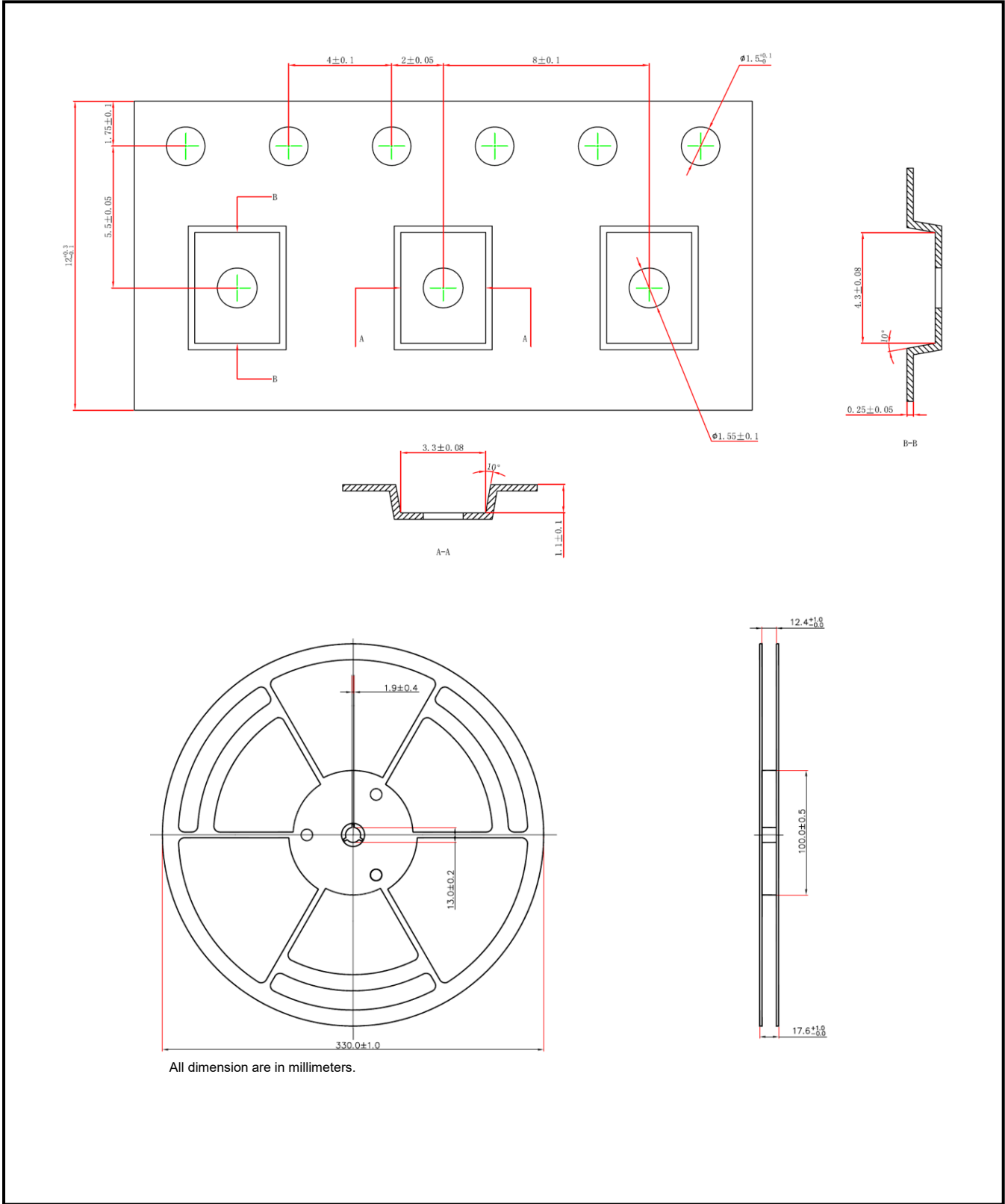
Marking Reference:



Die Orientation Dot
& Gate Position

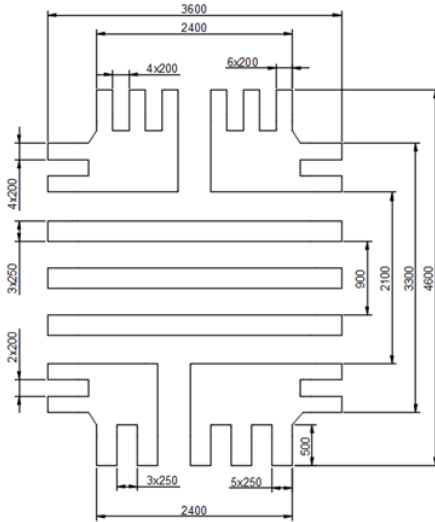
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot No	XXX
Row 5	Lot No	XXX

11. Reel Information



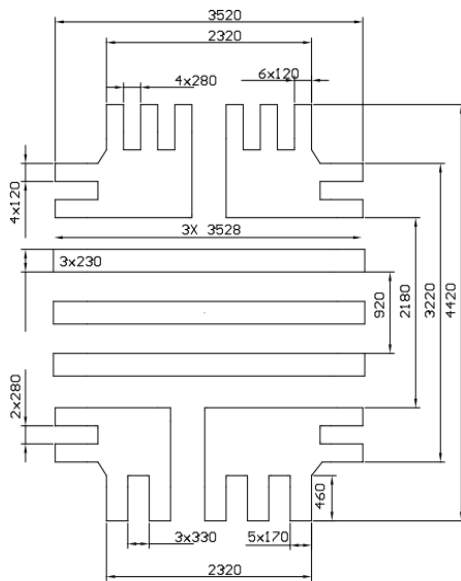
12. Land Pattern

Recommended Land Pattern



TOP VIEW Unit: μm

Recommended Stencil Drawing



TOP VIEW Unit: μm

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-12-12	1.0 version release
1.1	2022-12-22	Update package marking information
1.2	2023-07-21	Tighten I_{DSS} spec to 100uA from 200uA
1.3	2023-10-07	<ol style="list-style-type: none">1. Corrected typos2. Update package rendering on page13. Add Q_G max spec in Electric Characteristics
1.31	2023-11-08	Corrected typos

Important Notice

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